Comparison of the Trapezoidal Current and Stepped 2-Level Modulation Techniques in Modular DC-DC Converter

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Abstract

For high step-ratio connectivity in direct current (DC) grid applications, a modular (DC-DC) converter (MDCC) has been proposed. To improve the performance of the MDCC, this paper discusses a trapezoidal current modulation (TCM). Com-paring with stepped 2-level modulation where the sub-module (SM) capacitor voltages are balanced with a feedback control loop, TCM ensures the voltage balancing by applying an equal duty cycle for each SM in the high voltage stack with-out any additional feedback control. Three-level operation mode featured with large power transmission and high efficiency conversion, based on circulating current analysis and soft-switching performance is introduced. The control schemes of this operation mode is designed to minimize both the SM capacitor voltage ripples and the peak current. An analytical simulation of the MDCC is presented using MATLAB/SIMULINK to explain the operation and discuss the results.

Keywords- DC-DC converters, DC grids, dual active bridge, trapezoidal current mode.

I. INTRODUCTION

When the electric power system was first installed, direct current (DC) was superseded by alternating current (AC) [1], the ac transformer was the primary cause. However, the advancement of power electronics has allowed dc power systems to resurface. In the transmission of energy, DC provides significant advantages over alternating current, including smaller size of cables and lower power losses, and the elimination of peak voltages and reactive power. In addition, DC power is be-coming more prevalent in renewable energy systems like wind turbines and photovoltaic solar panels, as well as energy storage systems such as batteries and fuel cells, and in a variety of loads like modern home appliances, computers, data centers and electric cars. However, dc power grids adoption will take time, because dc power grids require the replacement of current ac network and still there is a gap between ac transformers and dc conversion technology, especially dc-dc converters for a high voltage range. The modular multilevel converter (MMC) discussed in [2] is now the suitable technology for high and medium voltage direct current systems, however it is mostly used to dc and ac systems interconnection, acting as rectifier or inverter. The development of medium voltage direct current and low voltage direct current grids, on the other hand, is of significant importance, therefore a DC-DC converter that provides a proper link between high voltage direct current, medium voltage direct current, and low voltage direct current systems will allow dc grids to be widely adopted. High efficiency, fault blocking, bidirectional power flow and voltage regulation should all be features of this converter [3], [4]. For dc-dc conversion, several MMCs have been proposed, but the front-to-front (FTF-MMC) is the preferred topology. Soft switching modulation (SS-MMC) and hard switching modulation (HS-MMC) are two different types of these topologies. By connecting two MMCs via a medium-frequency transformer, the hard switching topology generates multilevel ac voltages, however, it requires SM capacitor voltages balancing control, and the efficiency reduced by the hard-switching operation [5]–[11]. Soft switching topologies based on resonant tanks (R-MMC) [12]–[14] or triangular currents mode [15] have been proposed to solve this two problems, resulting in natural capacitor voltage balancing and soft switching. Despite its soft-switching operation, the resonant modular multilevel converter (R-MMC) it creates large peak currents and limits voltage regulation, resulting in high conduction losses that leads to reduce the efficiency. Stepped 2-level (S2L) modulation for MDCC with flexible design of the arm inductor is preferable solution that ensures lower circulating current, small SM capacitance value and use switching frequency equal to the fundamental frequency [16]. Trapezoidal current mode (TCM) used to DC-DC converters like dual active bridge (DAB), provides bidirectional power flow control with high efficiency while retaining zero current switching (ZCS) operation without applying resonance [17], [18]. As a result, trapezoidal current mode (TCM) considered the preferable solution for MDCCs, recently a triangular current mode was proposed to be used [15], which is a subset of TCM that achieves optimized soft switching. This paper discusses trapezoidal current mode TCM for high step ratio MDCC that minimizes peak current through the ac interconnection over triangular operation and pro-vides bidirectional power flow using an easy control method, SM capacitor voltages balancing and ZCS operation [15], and the results

of TCM method are compared with results obtained from S2L modulation. Section 2 shows topologies of the high-step ratio dc-dc MMC using TCM and dc/dc converter using S2L modulation, section 3 describes the proposed TCM method, section 4 discusses the power modeling, section 5 illustrate the control scheme, and in section 6 the simulation results of both modulation methods are reported and compared.

II. MDCC TOPOLOGIES

MDCC topology with high step ratio conversion is made up of a stack of series connected N half-bridge sub-modules (SM) that support the high-voltage (HV) side, an active full-bridge converter represents the connection of the low-voltage (LV) side, as shown in figure 1 [19].

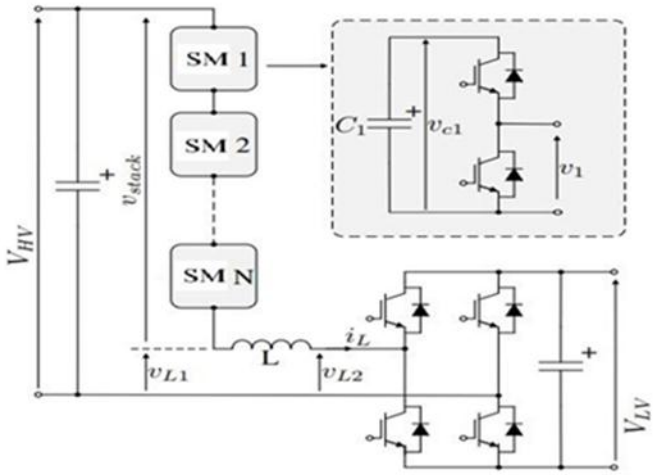

Figure 1. Topology of high step ratio MDCC with TCM.

The current flow through an inductor L that connects both subsystems is controlled to regulate bidirectional power transmission. The converter provides a high-step conversion ratio with no need to use a transformer, however for galvanic isolation a transformer might be added. To reduce voltage and current ripples filters are also used in both VH and LV sides, but for the simplicity, they are not taken into consideration in the following calculations. In Fig. 1 v_{L1} and v_{L2} are the voltages on both terminals of the inductor which considered in equations (1) and (2) that describe the overall operation of the converter, as show below

$$L\frac{di_L}{dt} = \underbrace{V_{HV} - \overbrace{\sum_{\iota=1}^{N} v_{c\iota} \cdot S_{\iota-HB}}^{v_{\text{stack}}}}_{v_{L1}} - i_L \cdot r_{eq} - \underbrace{V_{LV} \cdot S_{FB}}_{v_{L2}} \quad (1)$$

$$C_i\frac{dv_{ci}}{dt} = i_L \cdot S_{i-HB} \quad (2)$$

The inductor current can be regulated by the voltages v_{L1} and v_{L2}, as indicated in (3). The difference between the voltage of HV side and the stack voltage (v_{stack}), which is derived by summing the half-bridge output voltages v_i, is the voltage v_{L1}. As a result, stack voltage (v_{stack}) is determined by the switching states of each SM where Si-HB can be expressed in terms of commutation state Si-HB ϵ {1, 0}. v_{L2} is determined by the low voltage (LV) and the full-bridge switching state

$$L\frac{di_L}{dt} = v_{L1} - v_{L2} \quad (3)$$

Thus, the difference in voltages v_{L1} and v_{L2} on each side of the inductance L controls the current across it, allowing the power flow between both sides to be controlled. On other hand, the topology of the MDCC with S2L modulation is shown in figure 2 [22], it consists of two chain-links of N series connected SMs with an arm inductor L_a connected in series with the upper chain-link, these two chain-links work in pulse width modulation (PWM) with period T, the upper and lower chain-links with duty ratios (1-d) and d respectively. A circulating ac current must be pass between the chain-links to achieve the SM capacitors voltage balancing [22], therefore a shifted phase d_s generates between the signals that control the upper and lower chain links (v_{CL1} and v_{CL2}) as shown in figure 3[22].

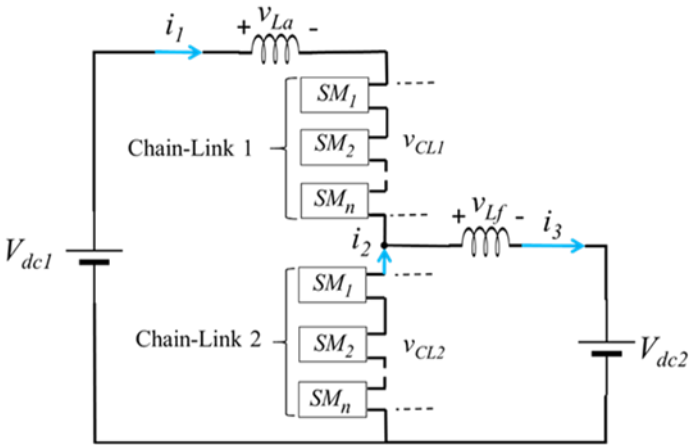

Figure 2. Topology of Buck type MDCC with S2L modulation.

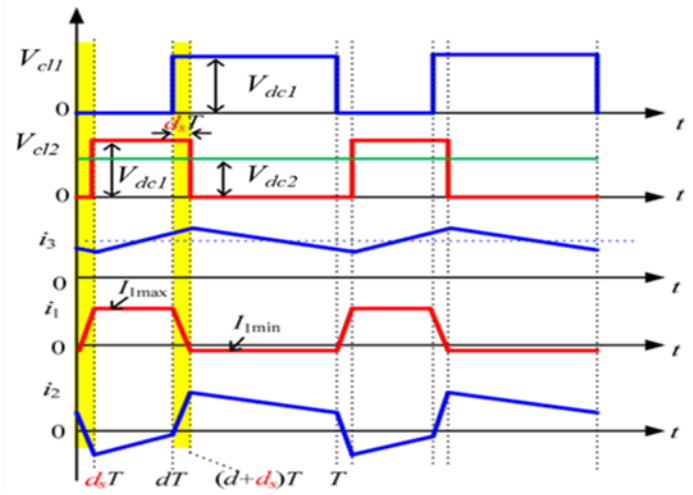

Figure 3. Waveforms of MDCC using S2L modulation.

III. TRAPEZOIDAL MODULATION

The voltages v_{L1} and v_{L2} must be adjusted to provide a three-level voltage waveform at each terminal of the inductor in order to produce a trapezoidal current. The full bridge uses unipolar modulation to generate three levels in v_{L2}, while the stack necessitates a one type of modulation to generate the required three levels in v_{L1}. To do this, the same waveform used for the SMs modulation with a Ts phase shift to increase the resulting frequency v_{L1} while maintaining SM capacitor voltages balance [15]. The output voltage of the first SM v_1 represents the repeating signal with a period of (N.Ts) dictated by the transition timings as illustrated in figure 4 [19]. If the SM capacitor voltages are balanced and equal to VC with a phase shift equal to Ts, a three level time-controlled voltage with an amplitude of V_C, center in (*N-1*). V_C and a period of *Ts* is formed in the stack called (v_{stack}) as expressed in (4)

$$v_{\text{stack}}(t) = \begin{cases} & 0 < t < t_1 \\ (N-1)V_C & t_3 < t < t_5 \\ & t_7 < t < T_s \\ \\ (N-2)V_C & t_1 < t < t_3 \\ N \cdot V_C & t_5 < t < t_7 \end{cases} \quad (4)$$

If (5) holds, v_{L1} is a three-level voltage with the same properties as v_{stack} but with a zero canter.

$$V_C = \frac{V_{HV}}{(N-1)} \tag{5}$$

Figure 4 illustrates the modulation waveforms presented for each SM, for example let $N = 5$. For the operation to be effective, all SMs must be healthy, in the event of a SM fails, V_C can be modified to the new number of SMs by bypassing the faulty SM. Using the stack modulation previously presented, the duty cycles (D_1, D_2, D_3 *and* D_4) of the voltages v_{L1}, v_{L2} could be managed with two additional phase-shift parameters Φ_1 and Φ_2 to generate a trapezoidal current across the inductor (Figs. 5(a), (b)) [19].

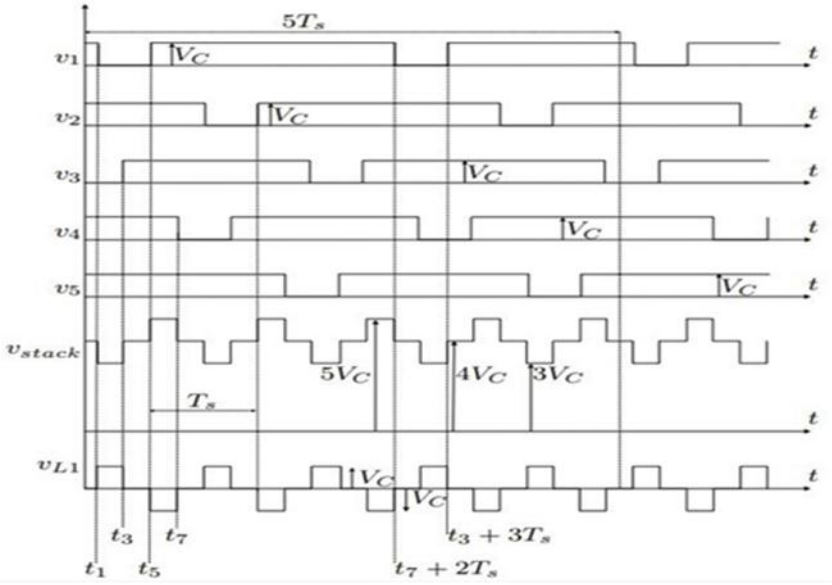

Figure 4. Waveforms in HV side for N=5 SMs and j=2.

Take into the consideration that the value of $D1$, D_3, $(\Phi_1 + D_2)$ and $(\Phi_2 + D_4)$ between 0 and 0.5, then the result waveform is defined in (6). This method of modulation enables multiple trapezoidal current waveforms to handle the same level of power, the extra degrees of freedom (Φ_1 and Φ_2) can reduces conduction losses and current peaks.

$$i_L(t) = \begin{cases} 0 & \text{if } t \in (0, t_1), (t_4, t_5) \\ & \vee\ (t_8, T_s) \\ \frac{V_C}{L}(t - t_1) & \text{if } t \in (t_1, t_2) \\ i(t_2) - \frac{V_{LV} - V_C}{L}(t - t_2) & \text{if } t \in (t_2, t_3) \\ i(t_3) - \frac{V_{LV}}{L}(t - t_3) & \text{if } t \in (t_3, t_4) \\ -\frac{V_C}{L}(t - t_4) & \text{if } t \in (t_5, t_6) \\ i(t_6) + \frac{V_{LV} - V_C}{L}(t - t_6) & \text{if } t \in (t_6, t_7) \\ i(t_7) + \frac{V_{LV}}{L}(t - t_7) & \text{if } t \in (t_7, t_8) \end{cases} \tag{6}$$

In trapezoidal current mode, equation (7) guarantees ZCS for half of the commutations. The peak currents in the inductor (8) are controlled by Φ_1 and Φ_2, allowing for current waveform optimization for a specified power transfer reference according to these variables.

$$D_{i+1} = r_V \cdot D_i \; i = 1{,}3 \tag{7}$$

$$i_L^{p1} = i_L(t_2) = \frac{V_C}{f_s L}\Phi_1$$

$$i_L^{p2} = i_L(t_6) = -\frac{V_C}{f_s L}\Phi_2 \tag{8}$$

r_V is the voltage ratio of the ac-link $r_V = \frac{V_{LV}}{r_S \cdot V_{HV}}$ (9)

Where r_S represents the stack modulation voltage ratio.

IV. POWER MODELING

The area covered by the inductor current in the first (A_{Ltp}^1) and second (A_{Ltp}^2) half cycles of the switching cycle is described in (10) and represented in Fig. 5(a) to model power exchange between the *HV* side, *LV* side and the SM stack. If the ZCS condition is achieved, these regions can be described as a function (f_{tp}) of the duty cycle D_i and phase shift Φ_i

$$\begin{aligned} A_{Ltp}^1 &= f_{tp}(\Phi_1, D_1) = \int_0^{\frac{T_s}{2}} i_L \cdot dt \\ A_{Ltp}^2 &= -f_{tp}(\Phi_2, D_3) = \int_{\frac{T_s}{2}}^{T_s} i_L \cdot dt \\ f_{tp}(\Phi, D) &= \frac{V_C \cdot D \cdot T}{2fL}\left(2\Phi - D(1 - r_V)\right) \end{aligned} \tag{10}$$

The sum of the areas A_{Ltp}^1 and A_{Ltp}^2 due to the inductor current waveform represents the average power delivered by HV side at one switching cycle P_{HV} which is the same as the HV side when neglecting the effect of the filters (11)

$$P_{HV} = V_{HV} \cdot \left(\frac{A_{Ltp}^1 + A_{Ltp}^2}{T_s}\right) \tag{11}$$

The previous analysis assumes during operation, the average voltage of the SM capacitor maintains balanced. The areas of the inductor current between times t_3 and t_4 (A_{Ltg}^1) and between times t_7 and t_8 (A_{Ltg}^2) are specified in (12) and represented in Fig. 5(a) to find the voltage capacitor balance condition. These areas can also be written as a function (f_{tg}) of the duty cycle D_i and phase shift Φ_i if the ZCS requirement is achieved.

$$\begin{aligned} A_{Ltg}^1 &= f_{tg}(\Phi_1, D_1) = \int_{t_3}^{t_4} i_L \cdot dt \\ A_{Ltg}^2 &= -f_{tg}(\Phi_2, D_3) = \int_{t_7}^{t_8} i_L \cdot dt \\ f_{tg}(\Phi, D) &= \frac{V_{LV} \cdot T}{2fL}\left(\Phi - D(1 - r_V)\right)^2 \end{aligned} \tag{12}$$

The SM capacitor voltage can be obtained by integrating the current passing through it, using the proposed modulation and trapezoidal current mode. Then, using the areas A_{Lpt}^1, A_{Lpt}^2, A_{Ltg}^1 and A_{Ltg}^2 to express the capacitor voltage during the modulation time ($N.T_s$) (13)

$$v_{ci}(t_0 + N \cdot T_s) = \quad v_{ci}(t_0) + \frac{A_{Ltp}^1 \cdot (N-2) + A_{Ltg}^1 + A_{Ltp}^2 \cdot N - A_{Ltg}^2}{C_i} \tag{13}$$

Therefore, the voltage balance condition state in the stack at steady sate in (14), the SM capacitor voltage must be constant in the modulation window ($N.T_s$).

$$A_{Ltp}^1 \cdot (N-2) + A_{Ltg}^1 + A_{Ltp}^2 \cdot N - A_{Ltg}^2 = 0 \tag{14}$$

As a result of solving (10) and (13) it is feasible to control the power flow while maintaining the capacitor voltage balance. As shown in Fig 5(b), if the phase shift of voltages v_{L1} and v_{L2} ($\Phi 1$ *and* $\Phi 2$) are inverted, negative power flow (from LV to HV side) same analysis can be carried out. Thus, these relationships provide full control for bidirectional power flow while maintaining the voltage balance and ZCS.

V. CONTROL SCHEME

Fig. 6 [20] shows the control scheme for the TCM, the voltage of LV regulated with PI controller to generate Φ1, Table 1 shows the equations to evaluate (Φ2, D1, D2, D3 and D4). Then, the phase shifted (Φ1 and Φ2) and the duty cycles (D1, D2, D3 and D4) used in the next block to evaluate both time vectors ti (t1, t3, t5 and t7) and tj (t2, t4, t6 and t8). The time vector ti applied to control the SMs of the stack block, while the time vector tj applied to control the full bridge block.

VI. Table 1. List of equations of the first block.

$\Phi_1 = \Phi_2$
$D_3 = \frac{1-\sigma}{2} - \frac{r_{S*P_{pu}}}{12*\sigma}, \sigma = 2.\Phi_1.r_v + 1 - r_v$
$D_1 + D_3 = r_v(1 - \Phi_1 - \Phi_2)$
$D1 = D_2.r_v, D_3 = D_4.r_v$

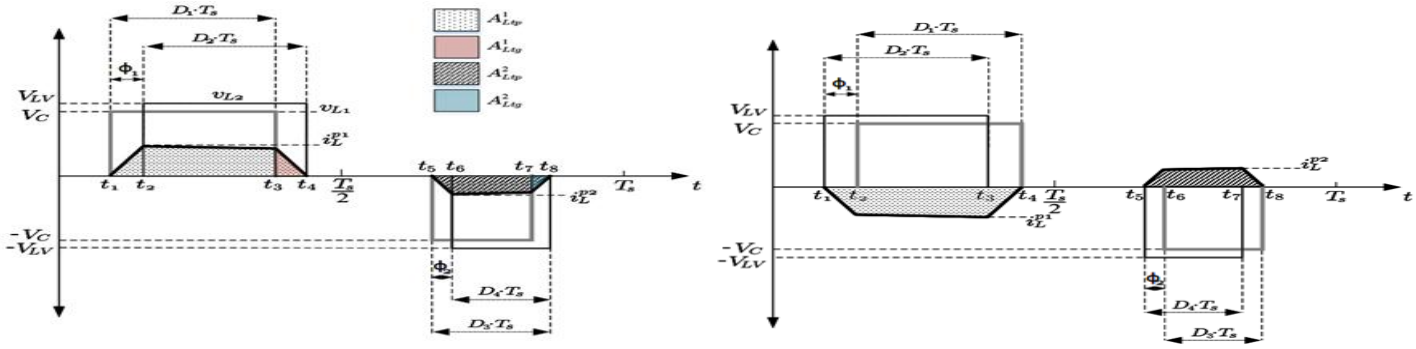

Figure 5. Current voltage waveforms for converter under trapezoidal modulation. (a) Power flow from HV side to LV side (b) Power flow from LV side to HV side.

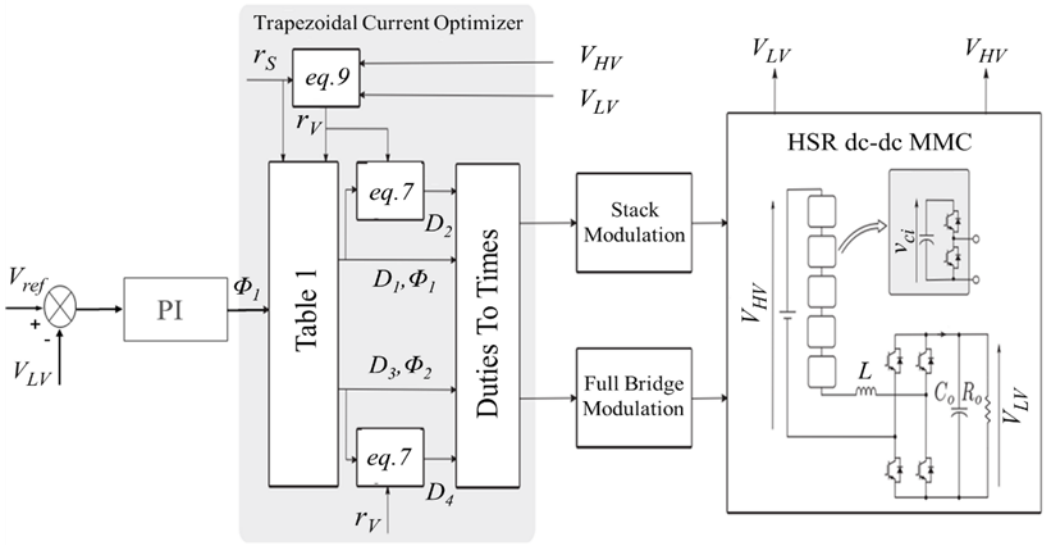

Figure 6**.** Proposed control scheme for the TCM.

VI. RESULTS

To verify the operation of the MDCC and achieve the voltage balancing of the SM capacitors using TCM, MATLAB/SIMULINK used to simulate the topology in Fig. 6 with parameters listed in Table 2 and compare these results with the results obtained in S2L modulation [22].

Table 2. Parameters of the simulated topology

Description	Parameters	Value
Transferred power	P_{pu}	800 kW
HV side voltage	H_{VH}	8 kV
LV side voltage	H_{LV}	2 kV
Number of SMs	N	5
Stack voltage ratio	r_s	0.25
Capacitance of SM capacitor	C_i	987 μF
Inductor inductance	L	811 μH
Output capacitance	C_o	987 μF
Output load	R_o	5 Ω
Switching frequency	f_s	5 kHz

A. Steady State Results

Figure 7 and figure 8 illustrate the steady state waveforms for both topologies. Figure 7 shows the waveforms of the ac-link v_{L1}, v_{L2} and i_L, the converter operates in TCM and four zero current switching are generated in each period T_s, the voltage in LV side regulated to 2 kV. Figure 8 [22] shows the waveform voltages of upper and lower chain link, the dotted box shows the transition period from which it clear to realize that these voltages are stepped 2-level and the output voltage is regulated to 2 kV.

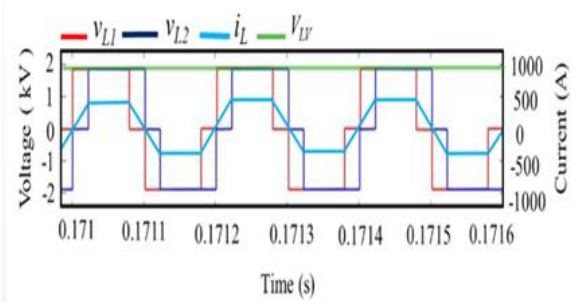

Figure 7. Steady-state waveforms of the ac-link using TCM.

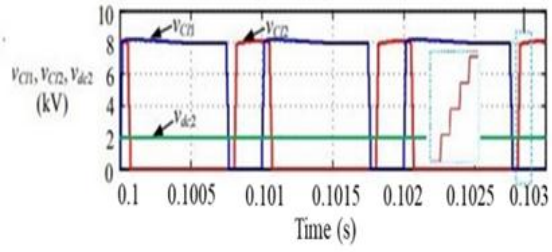

Figure 8. Steady-state waveforms using S2L modulation.

B. Dynamic Response

A step change in the load has been considered, at t = 0.25 sec the load stepped from half to full load for both topologies. In figure 9. where the dynamic waveforms of TCM, we can see the LV side has only undershoot about 7%, comparing with the waveform of output voltage of stepped 2-level modulation in figure 10 [22] which has overshoot and undershoot 8%, both systems return to the steady state in about 0.1 sec. The dotted boxes show the peaks of ac circulating current for both topologies.

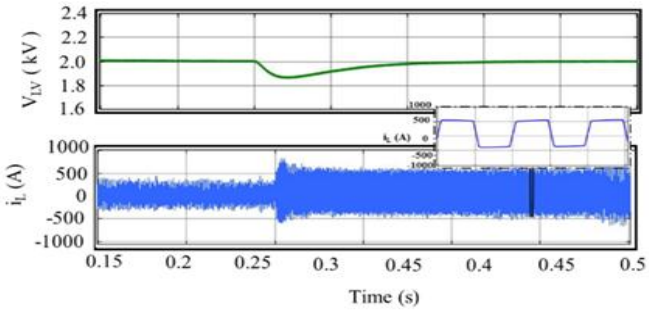

Figure 9. Dynamic-state waveforms using TCM.

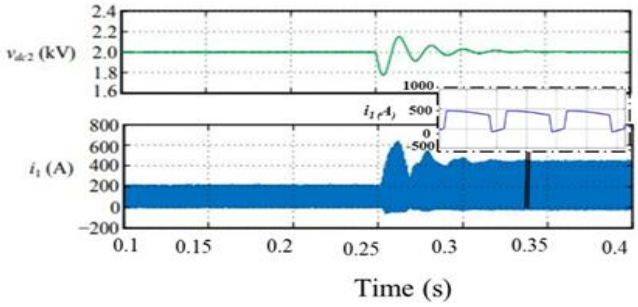

Figure 10. Dynamic-state waveforms using S2L modulation.

C. SM Capacitor Voltages Balancing

Figure 11. shows the waveform of the SM capacitor voltages using trapezoidal current mode which has been discussed in this paper, the voltage balancing is already achieved without the need to use a feedback control loop with voltage ripple 1%, while in S2L modulation method with a feedback control loop proposed to achieve the voltage balancing with voltage ripple 2% as shown in figure 12 [22].

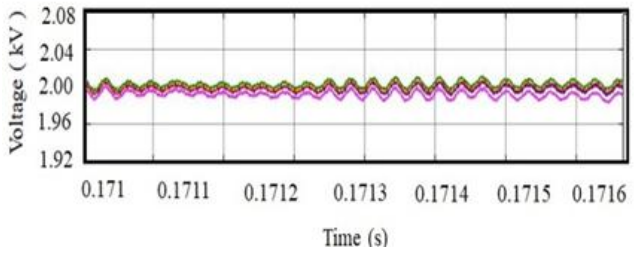

Figure 11. Waveforms of SM capacitor voltages (v_{c1}-v_{c5}) using TCM.

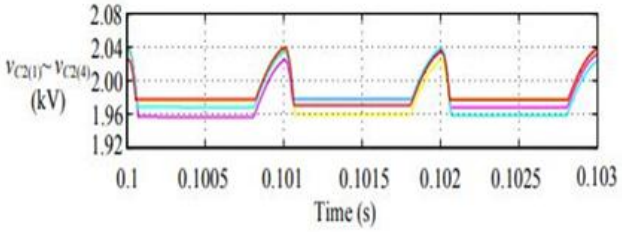

Figure 12. Waveforms of SM capacitor voltages (v_{c1}-v_{c4}) using S2L modulation.

VII. BRIEF COMPARISON BETWEEN THE TWO MODULATION TECHNIQUES

From the results obtained in the pervious section, a brief comparison between the TCM and S2L modulation Techniques can be illsutrated in the Table 3.

Table 3. Brief Comparison between the TCM and S2L Techniques

Modualtion Method	TCM	S2L
Voltage control balaning control	simple	complix
Output voltage regulation range	low	wide
SM capacitance value	large	small
Dynamic state overshoot	small	very small
Ripple of SM capacitor voltages	small	reduced to half

VIII. CONCLUSION

A trapezoidal current modulation TCM for high step conversion ratio has been discussed and compared with stepped 2-level modulation. This paper shows that TCM has advantages over stepped 2-level modulation characterized by use simple control method to control the output voltage and the SM capacitor voltages balancing achieved without use feedback control loop but has a drawback of low range of output voltage regulation, while the main advantages of stepped 2-level modulation are wide range of output voltage

regulation, small SM capacitance value and the switching frequency equal to the fundamental frequency with a disadvantage of requirement of a complex feedback control for SM capacitor voltages balancing .

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